REMARKS

The Examiner is thanked for the indication that claims 3-4 and 13 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-13 are pending in the application. Claims 1, 2, 9 and 12 are independent. By the foregoing Amendment, Applicants have amended claims 1, 2, 4, 5, 9, and 12. Applicants also have amended the Drawings. It is believed that these changes introduce no new matter and their entry is respectfully requested.

Objection to the Drawings

In the Office Action, the Examiner objected to the Drawings stating that Figure 1 should be labeled as "Prior Art" because only that which is old is shown. By the foregoing Amendment, Applicants have amended Figure 1 to accommodate the Examiner. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the objection to the Drawings.

Objection to Claim 4

In the Office Action, the Examiner objected to claim 4 citing a typographical error. By the foregoing Amendment, Applicants have amended claim 4 to depend from claim 3, which change accommodates the Examiner. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the objection to claim 4.

Rejection of Claims 2, 7-8, and 12 Under 35 U.S.C. §102(b)

In the Office Action, the Examiner rejected claims 2, 7-8, and 12 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,426,641 to Afrashteh et al. (hereinafter "Afrashteh"). A claim is anticipated only if each and every element of the claim is found in a reference. (MPEP §2131 *citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628 (Fed. Cir. 1987)). The identical invention must be shown in as complete detail as is contained in the claim. Id. *citing Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989)). Applicants respectfully traverse the rejection.

Amended claim 2 recites in pertinent part "circuitry merged with the RF power amplifier to apply a digital signal to the RF power amplifier, ***the digital signal to program a conduction angle of the RF power amplifier***" (emphasis added). Amended claim 12 recites in pertinent part "applying a digital signal to a radio frequency (RF) power amplifier; ***programming a conduction angle*** of the RF power amplifier ***using the digital signal***" (emphasis added). Support for the changes according to at least one embodiment can be found in Applicants' Specification at page 8, line 18 to page 9, line 5.

The Examiner states that claims 2 and 12 are clearly anticipated by Afrashteh. Applicants respectfully disagree and respectfully submit that Afrashteh fails to teach using a digital signal to program a conduction angle of the RF power amplifier as recited in amended claims 2 and/or 12. Applicants respectfully submit that although the internal clock 209 of Afrashteh determines when the amplifier 203 should be turned "off" after the transmission time-slot and signals the microprocessor 210 at a fixed time after each burst to again turn amplifier 203 "on," the purpose of turning the amplifier 203 "on" and "off" is "***to conserve power***" (emphasis added) (Afrashteh at column 15, line 60 to column 16, line 2) rather than to program a conduction angle and as Afrashteh specifically teaches at column 15, lines 25-27 "amplifier 203 is a conventional power amplifier, ***maintained in a class AB mode*** by means of selection of a quiescent point" "supplied on lead 205 during periods of no input signal" to the amplifier 203 from the antenna (emphasis added). Thus, Applicants respectfully submits that turning "on" and "off" of the amplifier 203 as taught by Afrashteh does not refer to controlling the conduction angle or the class of operation of the amplifier 203.

Applicants respectfully submit that because Afrashteh fails to teach the identical invention as recited in amended claims 2 and 12, amended claims 2 and 12 are patentable over Afrashteh. Applicants respectfully submit further that claims 7-8 properly depend from claim 2 and are thus patentable over Afrashteh for at least the same reasons that claim 2 is patentable over Afrashteh. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection of claims 2, 7-8, and 12.

Rejection of Claims 1 and 9-10 Under 35 U.S.C. §102(e)

In the Office Action, the Examiner rejected claims 1 and 9-10 as being anticipated by U.S. Patent No. 6,542,037 B2 to Noll et al. (hereinafter "Noll"). Applicants respectfully traverse the rejection.

Amended claim 1 recites in pertinent part "the drain of the first transistor ***directly connected*** to the sources of the second and third transistors and, the drain of the second transistor ***directly connected*** to the gate of the second transistor via the first resistor, the gate of the second transistor ***directly connected*** to the gate of the sixth transistor via the second resistor, the drain of the fourth transistor ***directly connected*** to the sources of the fifth and sixth transistors and, the drain of the fifth transistor ***directly connected*** to the gate of the fifth transistor via the third resistor, the gate of the fifth transistor ***directly connected*** to the gate of the third transistor via the fourth resistor, the fourth resistor ***directly connected*** to the gate of the third transistor and the second resistor ***directly connected*** to the gate of the sixth transistor" (emphasis added). Support for these changes according to at least one embodiment can be found in Applicants' Specification at page 6, lines 1-7, page 6 line, 25 to page 7, line 2, and in Figure 5.

Amended claim 9 recites in pertinent part "a self-biased cascode stage coupled to the driver stage, the self-biased cascode stage including a first transistor, a second transistor, a third transistor, a fourth transistor, a fifth transistor, and a sixth transistor, each having a drain, a source, and a gate, the drain of the first transistor ***directly connected*** to the sources of the second and third transistors, the gate of the first transistor ***directly connected*** to the driver stage, the drain of the second transistor ***directly connected*** to the gate of the second transistor via the first resistor, and the gate of the second transistor ***directly connected*** to the gate of the fifth transistor via the second resistor" (emphasis added). Support for these changes according to at least one embodiment can be found in Applicants' Specification at page 6, lines 1-7, page 6 line, 25 to page 7, line 2, and in Figure 5.

The Examiner states that the terminals of the transistors in Noll are connected to other terminals via intermediate elements such as capacitors and other transistors. Applicants respectfully submit, however, that Noll fails to teach the identical self-biased cascode stage as

recited in amended claims 1 and 9. Applicants respectfully submit that because Noll fails to teach the identical invention as recited in amended claims 1 and 9 that claims 1 and 9 are patentable over Noll. Applicants respectfully submit further that claim 10 properly depends from claim 9 and is thus patentable over Noll for at least the same reasons that claim 9 is patentable over Noll. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection of claims 1 and 9-10.

Rejection of Claims 5-6 Under 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected claims 5-6 under 35 U.S.C. § 103(a) as being unpatentable over Afrashteh in view of U.S. Patent Publication No.2002/0196086 to Sowalti (hereinafter "Sowalti"). To establish a *prima facie* case of obviousness, an Examiner must show three things: (1) that there is some suggestion or motivation to modify a reference or combine reference teachings to arrive at the claimed invention, (2) that there must be a reasonable expectation of success, and (3) that the references teach or suggest each and every element of the claimed invention. MPEP §2143. In combining references, the Examiner must use a legitimate rationale as to why one would be motivated to combine the references. MPEP §2144. One such legitimate rationale is "art recognized equivalence for the same purpose. MPEP §2144.06. In order to rely on this rationale to support an obviousness rejection, however, the equivalency must be recognized in the prior art, and cannot be based on Applicant's disclosure or the mere fact that the components at issue are functional or mechanical equivalents. MPEP §2144.06. Applicants respectfully traverse the rejection.

In the Office Action, the Examiner makes several assertions:

(1) Afrashteh is silent as to the details of its RF power amplifier;

(2) Self-biased cascode stage amplifiers are conventional in the art for use a RF power amplifiers; and

(3) Sowalti teaches various cascode stage self-biased power amplifiers.

The Examiner then concludes that it would have been obvious to have replaced the RF power amplifier in Afrashteh with a self-biased cascode stage RF power amplifier because one would be motivated to use any art-recognized equivalent RF power amplifier stage, such as the

conventional self-biased cascode RF power amplifier shown in Sowalti. Applicants respectfully disagree.

Sowalti appears to teach a cascode stage consisting of a single cascode arrangement, primarily of M1 and M2. In contrast, amended claim 5 recites in pertinent part "wherein the RF power amplifier includes a self-biased ***differential cross-coupled*** cascode stage" (emphasis added). Support for these changes can be found in Figure 5 and such an arrangement according to an embodiment was included in at least original claim 1, thus no new search is required. Thus as a first matter, Applicants respectfully submit that the Examiner has not shown how the arrangement of Sowalti would be considered an art-recognized mechanical or structural equivalent of the differential cascode cross-coupled cascode circuitry 500 of the present invention.

As a second matter, Applicants respectfully submit that the arrangement of Sowalti and the differential cascode cross-coupled cascode circuitry 500 of the present invention are not functional equivalents either. For example, the circuit in Sowalti is characterized by a high resistance signal path both when M1 is "on" and when M1 is "off." In contrast, the differential cascode cross-coupled cascode circuitry 500 of the present invention creates a lower resistance signal path through the transistor 506. This is characterized as a low resistance signal path because as the voltage in one signal path is going up the voltage in the other signal path is going down. When the transistor 502 is on, the overall on-resistance in the signal path that goes through the transistors 502, 504, and 506 is small because of the cross-coupled configuration of the transistor 506. Such a configuration biases the gate of the transistor 514 high. Thus, when the transistor 502 is on, the gate of the transistor 506 also is biased high. When the overall resistance is reduced, the circuit is more efficient.

Moreover, the resistors 508, 510, 518, and 520 provide a self-biasing feature for the circuit 500 to control the maximum gate-drain voltage for the transistor 504 when the transistor 502 is off, the maximum gate-drain voltage for the transistor 502 when the transistor 502 is off, and the maximum gate-source voltage for the transistors 506 when the transistor 502 is on. The arrow 605 in the present invention illustrates that the voltage swing in the circuit 500 is approximately V_{DD} as opposed to more than twice V_{DD}, as is the case with Sowalti. This small

voltage swing ensures that the transistors 502, 504, and 506 all operate below the breakdown voltage limitations while power efficiency is simultaneously improved. The functions of claim 5 and Sowalti, therefore, would not be considered art-recognized equivalents.

As a third matter, Applicants respectfully point out that the only mention of using a self-biased differential cascode cross-coupled cascode circuitry in an RF power amplifier is in Applicants' Specification, which Applicants respectfully submit in not a proper source for establishing an art-recognized equivalent.

Applicants respectfully submit that because the Examiner has failed to provide sufficient support for an art-recognized equivalents rationale the Examiner cannot rely on that rationale to support the obviousness rejection. Applicants, therefore, respectfully submit that the Examiner has failed to make a prima facie case of obviousness with respect to claim 5 and that claim 5 is thus patentable over Afrashteh in view Sowalti. Applicants respectfully submit further that claim 6 properly depends from claim 5 and is thus patentable over Afrashteh in view Sowalti for at least the same reasons that claim 5 is patentable over Afrashteh in view Sowalti. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection of claims 5 and 6.

CONCLUSION

Applicants submit that all grounds for rejection have been properly traversed or accommodated, and that the application is in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 1/13/2005

Jan Little-Washington
Reg. No. 41,181
(206) 292-8600

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on January 13, 2005
Date of Deposit

Adrian Villarreal
Name of Person Mailing Correspondence

Signature

January 13, 2005
Date

DRAWING AMENDMENTS

The attached sheet of drawings includes changes to Figure 1. This sheet, which includes Figures 1, 2, and 3, replaces the original sheet including Figures 1, 2, and 3. Figure 1 has been labeled "Prior Art."

Attachment: Replacement Sheet

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PRIOR ART

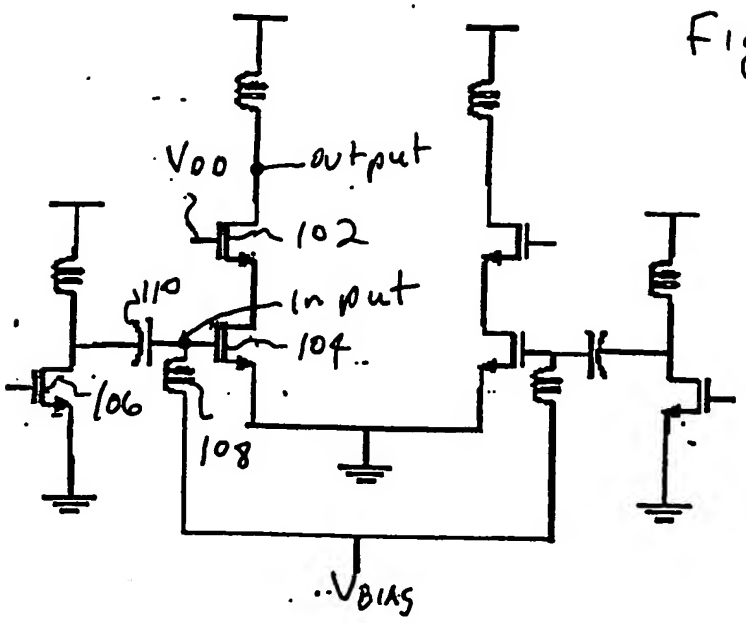

Figure 1

100

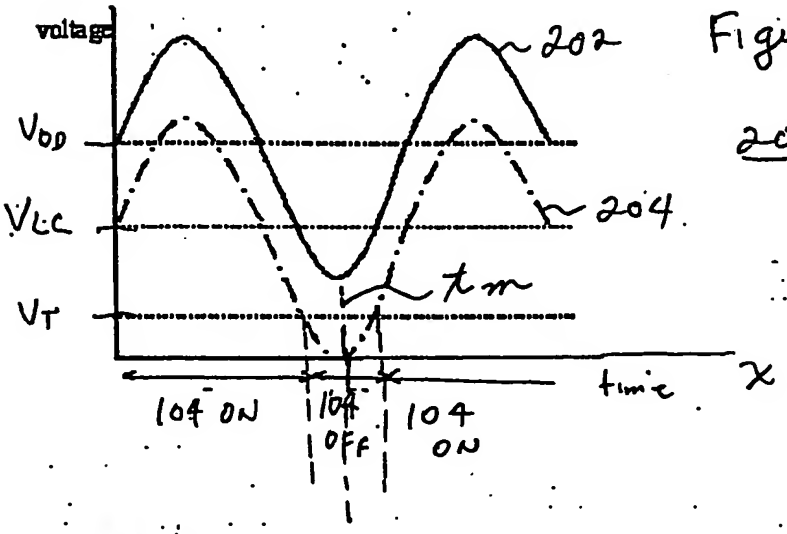

Figure 2

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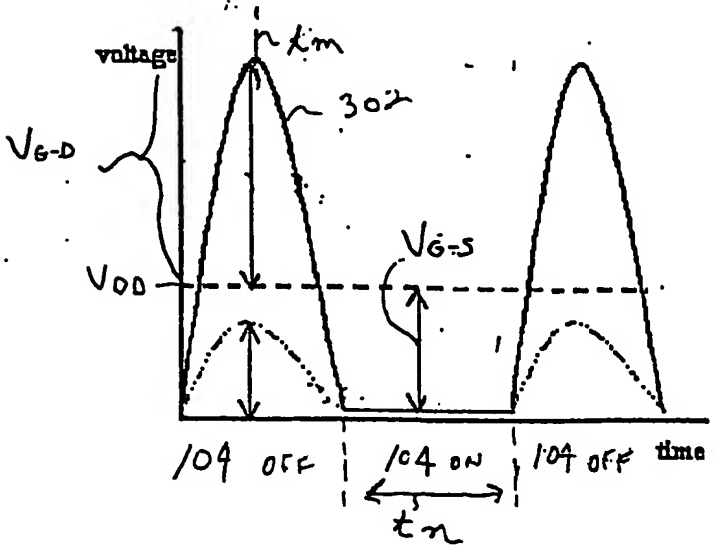

Figure 3

300